SAU-XDS510-USB Lite
JTAG Emulator

User's Guide

2014.

Contents

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About This Manual

This manual describes SAU-XDS510-USB Lite JTAG emulator designed for being used in combination with digital signal processors (DSPs) and microcontrollers manufactured by Texas Instruments Incorporated (TI). SAU-XDS510-USB Lite JTAG Emulator is a portable table top device attached to a personal computer or a laptop. It allows to develop and debug applications based on DSPs and microcontrollers from TI.

1. Introduction to SAU-XDS510-USB Lite JTAG Emulator

This chapter provides a description of SAU-XDS510-USB Lite JTAG Emulator and its key features.

1.1 Overview of SAU-XDS510-USB Lite JTAG Emulator

SAU-XDS510-USB Lite JTAG Emulator was designed for being used with digital signal processors (DSPs) and microprocessors that are connected through JTAG. The Emulator supports connection through JTAG at the levels of +1.65 … +3.3 volt (5V tolerant). The Emulator is connected to a PC using USB-interface and draws no power from the target system.
Figure 1-1 shows the SAU-XDS510-USB Lite JTAG Emulator.
SAU-XDS510-USB Lite JTAG Emulator set contains:

- SAU-XDS510-USB Lite JTAG emulator.
- 3 adapters (14-pin TI, 20-pin CTI and 20-pin ARM).
- CD-ROM with drivers.

Figure 1-1. SAU-XDS510-USB Lite JTAG Emulator

SAU-XDS510-USB Lite is designed to be compatible with the existing debuggers provided by Texas Instruments.

1.2 Key Features of SAU-XDS510-USB Lite JTAG Emulator

SAU-XDS510-USB Lite JTAG Emulator has the following features:

- Supports Texas Instruments digital signal processors, processors and microcontrollers (C2000 (including LF24xx and F24x), C5000, C6000, ARM7, ARM9, ARM11, Cortex-A, Cortex-R, Cortex-M, DaVinci, OMAP, Sitara, Tegra, Integra, Keystone, Piccolo, Delfino, Hercules, Stellaris, Tiva, TMS470, TMS570, RM4, etc.), TMS320VC33. It also supports any multicores and/or multiprocessors combinations of listed above cores and processors both placed into one chip and connected in one JTAG chain in device with possibility of connection other devices (e.g. FPGA) in this chain.
- Ultra-miniature design (smallest XDS510 class emulator of currently produced): emulation controller with buffers is placed inside of connector body. It allowed to eliminate JTAG tail which significantly improved JTAG signal quality and connection stability in EMI conditions.
- Acceleration is up to 1.3 times versus Iso Plus emulator (emulation controller similar to the one used in Iso Plus V.2).
- Works with higher clock frequencies TCK without "fine tuning" (up to 52.5MHz depending on debugging device).
- Supports from +1.65 volt up to +3.3 volt JTAG interfaces (5V tolerant).
- Controlled JTAG signal level for work with interfaces with high PD signal level.
- Tight JTAG signal level setting independent from PD level.
- Compatible with Texas Instruments XDS510 emulator.
- Advanced JTAG controller (SAU V.2) enables high emulation performance.
- Compatible with USB 1.1 and USB 2.0 (high speed, full speed).
- Drastic boost performance when connected via USB 3.0 (depending on host controller type and his driver).
- While connected to PC via USB no additional power source is required.
- Three color status and mode LED indicator.
- Supports programming and configuring FPGA and CPLD through SVF player (SVF Specification Rev. E + Lattice Semiconductor enhancements).
- Supports internal and external in-circuit supported processors memory programming through SauFlash/TCLXDS utility shipped with drivers.
- Supports Adaptive Clocking without additional adapters.
- Flexible TCK frequency adjustment.
- Possible to work from target TCK source (from TCKR (TCK_RET)).
- Possible to work without TCKR (TCK_RET) signal.
- Supports JTAG signal buffering including registers clocking TCK buffering.
- Compatible with Texas Instruments Code Composer IDE (v 4.10 for TMS320C3x/4x) and Code Composer Studio IDE (all versions).
- Compatible with Microsoft Windows 2000, Windows XP, Windows Vista (32-bit, 64-bit), Windows 7, Windows 8, Windows 8.1, Windows Server.
- Compatible with Linux (full technical support for RHEL, Centos, Fedora distributions, consultative for others).

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1.3 Key Items of SAU-XDS510-USB Lite JTAG Emulator

SAU-XDS510-USB Lite view is shown in Figure 1-2.

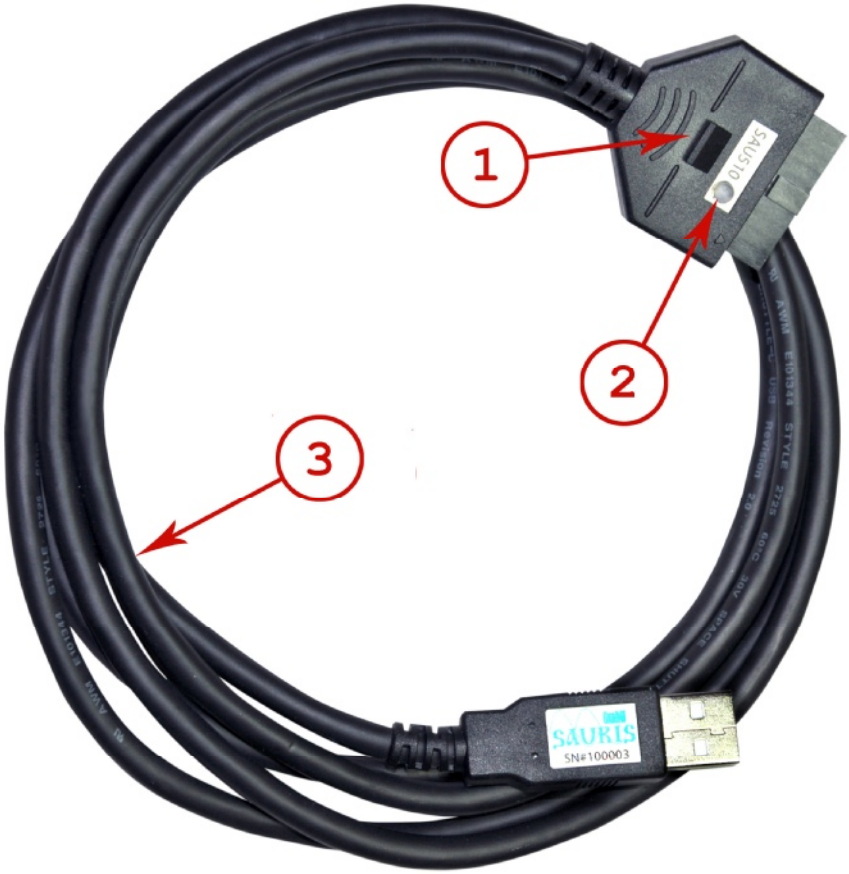


Figure 1-2. SAU-XDS510-USB Lite JTAG emulator

Key items are:

1. Emulator with JTAG connector.
2. 3 color status LED indicator.
3. USB cable.

2. SAU-XDS510-USB Lite JTAG Emulator Plugging

This chapter helps you to plug SAU-XDS510-USB Lite JTAG Emulator into your system.

Note: you should have Code Composer Studio installed before installing SAU-XDS510-USB Lite

In order to use specific software packages such as the Code Composer Studio from TI refer to the manufacturer's documentation.

2.1. Equipment required

The lists below include the equipment and software required for SAU-XDS510-USB Lite JTAG emulator operation.

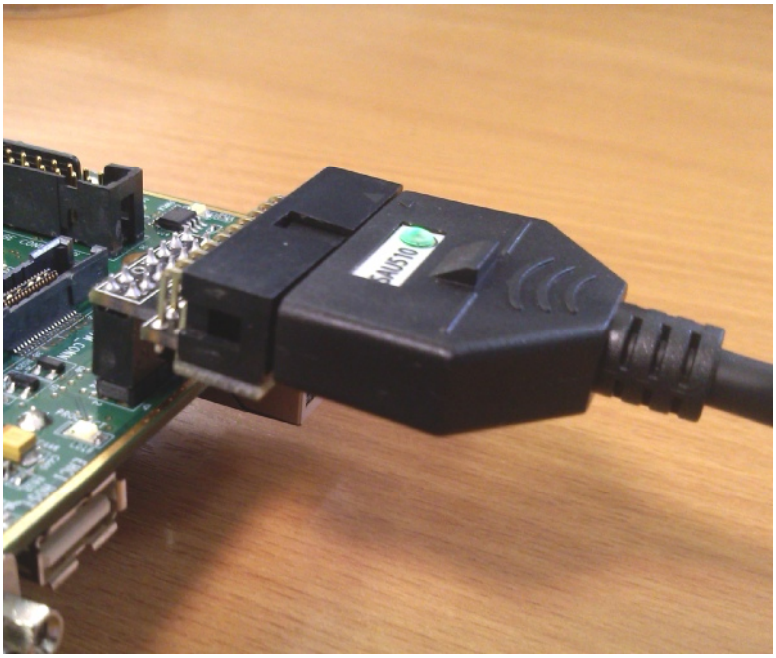
Hardware checklist.

- **Host:** any PC or laptop with a hard-disk system and a USB port and a CD-ROM disk drive.
- **Memory:** minimum of 32MB.
- **Display:** color VGA or LCD.
- **Emulator:** SAU-XDS510-USB Lite JTAG emulator.
- **Target system:** any TI DSP-based or TI Microcontroller-based board with power supply.
- **Connectors:** 14-pin connector (two rows of seven pins), 20-pin connector ARM JTAG or 20-pin CTI JTAG.See Section 3 for more information on connecting to target system

Software checklist.

- **Operating system:** Microsoft Windows 2000, Windows XP, Windows Vista (32-bit, 64-bit), Windows 7, Windows 8, Windows 8.1, Windows Server (32,64-bit), Linux.
- **Software tools:** Code Composer Studio.
- **Drivers:** Sauris GmbH drivers for TI Code Composer Studio (are included into SAU-XDS510-USB Lite JTAG emulator delivery set and are also available at Sauris GmbH website – www.sauris.de).

2.2. Connecting SAU510-USB ISO PLUS JTAG v.2 Emulator



Follow the steps in this section to plug SAU-XDS510-USB Lite Emulator in your PC and target board. Figure 2-1 shows SAU-XDS510-USB Lite connected to a target system and a PC. While using standard 14-pin TI JTAG connector it is possible to connect SAU-XDS510-USB Lite without adapter, aligning connectors first contacts.

Follow these steps to connect SAU-XDS510-USB Lite emulator:

1. Turn off all antivirus software on your PC.

2. Insert the Sauris GmbH USB Driver CD in the computer CD-ROM drive.

Figure 2-1. Connecting SAU-XDS510-USB Lite

3. The installer starts automatically if autoplay is turned on. If it doesn't, open the CD with the drivers in the File Manager window and run CD:\Windows\sau510usb_Install.exe and follow the instructions on the screen.

4. Turn on the antivirus software if needed.

5. Connect your SAU-XDS510-USB Lite JTAG emulator USB cable to PC.

6. After a while Windows will detect a new hardware and prompt you with «New Hardware Found» screen. If you want to verify the USB driver installation has been successful, right click Control Panel and select Properties→Hardware→Device Manager. You should see a new class JTAG Emulator and one emulator (SAU-XDS510-USB Lite JTAG emulator) installed.

7. Connect the emulator to the JTAG on your target board.

In future, after the drivers are installed, follow these steps to connect SAU-XDS510-USB Lite JTAG emulator:

1. Turn off the power supply of your target board.
2. Connect the emulator's JTAG connector to your target board.
3. Connect SAU-XDS510-USB Lite JTAG emulator's USB-cable to PC.
4. Apply power to the target board.

Detach SAU-XDS510-USB Lite JTAG emulator in the reverse order:

1. Turn off the power supply of your target board.
2. Detach SAU-XDS510-USB Lite JTAG emulator's USB-cable from PC.
3. Detach the emulator's JTAG connector from your target board.

Note: Be very careful with the target cable connectors. Connect them gently; do not force them into position, or you may damage the connectors.

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2.3. SAU-XDS510-USB Lite LED

SAU-XDS510-USB Lite emulator has a three color indicator. This indicator shows emulator working modes. USB High speed (480 Mbps) mode* color values are shown in table:

Figure 2-2. LED Indicator

Color	Description
Red	• **lights** - TRST signal is active (JTAG is in reset). TRST is activated when a target board power downs and by PC command (for example while all connections are closed) • **short blink** - USB power is on, but emulator is not configured.
Green	• **short blink** - there is no power on target. • **lights** - there is a power on target. • **blinks evenly** - there is a power on target, but there is no return clock signal (TCK_RET)
Blue	• PC is exchanging data with emulator

* If USB connected as Full Speed (12 Mbps), then green and blue are reversed

3. Specifications for Your Target System's Connection to the Emulator

This chapter contains the information on connecting your target system to the emulator. Your target system must have a special 14-pin connector JTAG, 20-pin ARM JTAG or 20-pin CTI JTAG for proper communication with the emulator.

3.1. Designing Your Target System's JTAG Connector

The emulator is connected to target systems through a dedicated port. The port supports IEEE 1149.1 (JTAG) standard and is accessible through the emulator. The board is to have a 20-pin header (2 rows of 7 pins), 20-pin ARM header or 20-pin CTI header in order to communicate with the emulator.

NOTE: Emulator outputs voltage level can be changed from 1.65 to 3.3V. Check paragraph 3.6.8 for details.

3.1.1. 14-pin JTAG description

The pin assignment scheme is shown in Figure 3-1. And the emulation signals are described in Table 1.

TMS	1	2	TRST-
TDI	3	4	GND
PD(Vcc)	5	6	No pin (key)
TDO	7	8	GND
TCK_RET	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1

Figure 3-1. 14-pin JTAG Connector

Table 1. 14-Pin Header Signal Description

Pin #	Signal	Description	Emulator State	Target State
1	TMS	JTAG test mode selection	Output	Input
2	TRST-	JTAG test reset	Output	Input
3	TDI	JTAG test data input.	Output	Input
5	PD	Presence detect. Indicates power and voltage levels on JTAG signal circuits. It should be connected to target JTAG I/O buffers.	Input	Output
7	TDO	JTAG test data output.	Input	Output
9	TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output
11	TCK	JTAG test clock. TCK is a 12-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
13	EMU0	Emulation pin 0.	Input/Output	Input/Output
14	EMU1	Emulation pin 1.	Input/Output	Input/Output

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3.1.2. 20-pin ARM JTAG description

The pin assignment scheme is shown in Figure 3-2. And the emulation signals are described in Table 2.

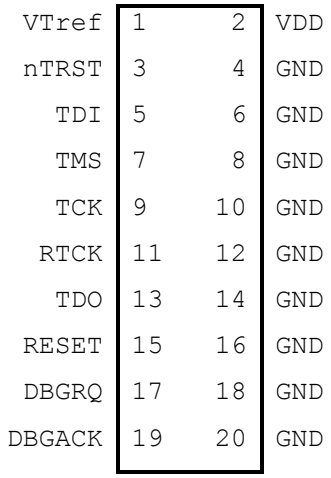

Figure 3-2. 20-pin ARM JTAG Connector

Table 2. 20-Pin ARM Header Signal Description

Pin #	Signal	Description	Emulator State	Target State
1	VTref	Power detect. Indicates power and voltage levels on JTAG signal circuits. It should be connected to target JTAG I/O buffers.	Input	Output
2	VDD	Power	NC	-
3	nTRST	JTAG Reset	Output	Input
5	TDI	JTAG data input of the target CPU	Output	Input
7	TMS	JTAG mode set input of the target CPU	Output	Input
9	TCK	JTAG clock signal to target CPU.	Output	Input
11	RTCK	Return test clock signal from the target	Input	Output
13	TDO	JTAG data output from the target CPU.	Input	Output
15	RESET	Target CPU reset signal	Input/Output	Input/Output
17	DBGRQ	Debug request signal	NC	Input
19	DBGACK	Debug acknowledgement signal	NC	Output

3.1.3. 20-pin CTI JTAG description

The pin assignment scheme is shown in Figure 3-3. And the emulation signals are described in Table 3.

TMS	1	2	TRST-
TDI	3	4	GND
PD	5	6	No pin (key)
TDO	7	8	GND
TCK_RET	9	10	GND
TCK	11	12	GND
EMU0	13	14	EMU1
SRST	15	16	GND
EMU2	17	18	EMU3
EMU4	19	20	GND

Figure 3-3. 20-pin CTI JTAG Connector

Table 3. 20-Pin CTI Header Signal Description

Pin #	Signal	Description	Emulator State	Target State
1	TMS	JTAG test mode selection	Output	Input
2	TRST-	JTAG test reset	Output	Input
3	TDI	JTAG test data input.	Output	Input
5	PD	Power detect. Indicates power and voltage levels on JTAG signal circuits. It should be connected to target JTAG I/O buffers.	Input	Output
7	TDO	JTAG test data output.	Input	Output
9	TCK_RET	JTAG test clock return. Test clock input to the emulator. May be a buffered or unbuffered version of TCK.	Input	Output
11	TCK	JTAG test clock. TCK is a 12-MHz clock source from the emulation pod. This signal can be used to drive the system test clock.	Output	Input
13	EMU0	Emulation pin 0.	Input/Output	Input/Output
14	EMU1	Emulation pin 1.	Input/Output	Input/Output
15	SRST	This is the target reference voltage. It is used to check if the target has power, to create the logic-level reference for the input comparators and to control the output logic levels to the target. It is normally fed from Vdd of the target board and must not have a series resistor.	Open drain	Input/Output
17	EMU2	This pin is not connected	Input/Output	Input/Output
18	EMU3	JTAG Reset	Input/Output	Input/Output
19	EMU4	JTAG data input of the target CPU	Input/Output	Input/Output

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3.2. Bus Protocol

The IEEE 1149.1 specification covers the requirements for JTAG bus of the target devices (such as the TMS320C6000 family) and provides certain rules summarized as follows:

- The TMS/TDI inputs are sampled on the rising edge of the device TCK signal.
- The TDO output is clocked from the falling edge of the device TCK signal.

When JTAG devices are daisy-chained together, the TDO from each of the devices in the chain has a definite period in the TCK cycle. Such synchronization scheme allows to distinguish the data from different target devices included into the same chain. The penalty for this timing scheme is a reduced TCK frequency. The IEEE 1149.1 specification does not provide rules for JTAG bus master devices (e.g. emulator).

3.3. Emulator Cable Pod Logic

SAU-XDS510-USB Lite emulator set contains three adapters: 14-pin TI JTAG, 20-pin CTI JTAG and 20-pin ARM. Figure 3-4 shows the emulator with 14-pin TI JTAG adapter. In case of there is a free space on pcb it is possible to connect emulator directly, without using adapter (Figure 3-5). Key features of JTAG interface:

- TMS and TDI signals are generated from the rising edge of TCK_RET, on default (but the standard can be adjusted in the configuration file).
- The edges of TMS, TDI, TCK and TRST signals do not coincide in order to reduce signal echo.
- TCK equals 15-MHz on default. You may also set another level of TCK.

Figure. 3-4. Emulator with adapter

Figure. 3-5. Emulator without adapter

3.4. Emulator Cable Pod Signal Timing

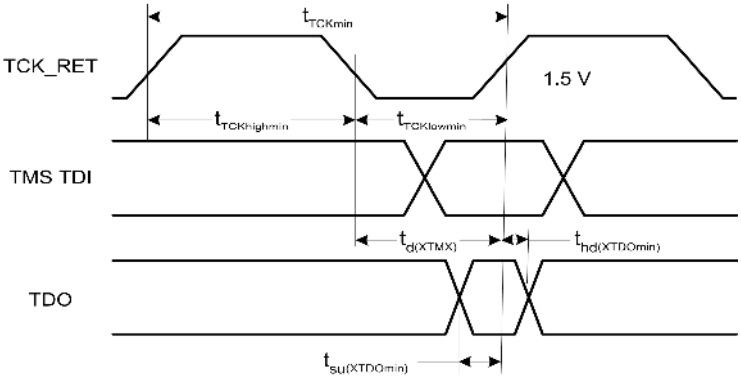

Figure 3-6. Signal Timings for the Emulator

Figure 3-6 shows the clock signal timings for the emulator. Table 4 defines the timing parameters for the emulator. The timing parameters are for reference only, Sauris GmbH has not tested them and doesn't guarantee their coincidence with the given in the table. The emulator pod uses TCK_RET as its clock source for internal synchronization. TCK can also be used as an optional test clock source for the target system.

Table 4. Emulator Pod Timing Parameters

No	Reference	Description	Min	Max	Units
1	t_{TCKmin}	TCK_RET period	19	-	ns
2	$t_{TCKhighmin}$	TCK_RET high pulse duration	9	-	ns
3	$t_{TCKlowmin}$	TCK_RET low pulse duration	9	-	ns
4	$t_{d(XTMX)}$	TMS/TDI setting time after TCK_RET edge*	1,7	9,5	ns
5	$t_{su(XTDOmin)}$	TDO setup time to TCK_RET high	2		ns
6	$t_{hd(XTDOmin)}$	TDO hold time from TCK_RET high	-0,5		ns

* from positive edge of TCK_RET (if POD_TDOONTCKFALL=NO) and from negative edge of TMS/TDI (if POD_TDOONTCKFALL=YES).

3.5. Buffering Signals Between the Emulator and the Target System

It is extremely important to provide high-quality signals between the emulator and the target system, especially the processor TCK and the emulator TCK_RET signals. In some cases this may require special PCB trace routing and using termination resistors to match the trace impedance. If the distance between the emulation header and the target device is longer than 15 cm, the emulation signals must be buffered. The need for signal buffering can be divided in two cases:

- **No signal buffering.** As shown in figure 3-6, the distance between the header and the target device does not exceed 15 cm.
- **Buffered emulation signals.** Figure 3-7 shows that the distance between the emulation header and the target device is longer than 15 cm. The target device signals TMS, TDI, TDO, and TCK_RET are buffered through several additional units.

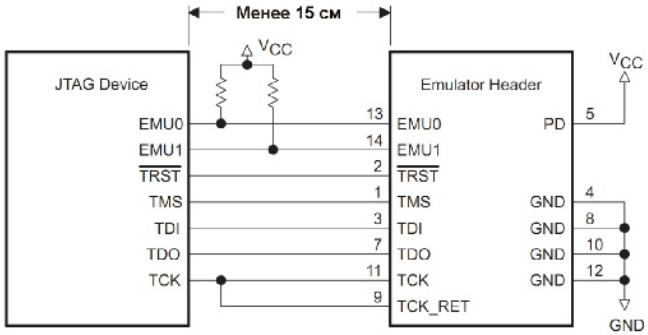

Figure 3-7. No Signal Buffering

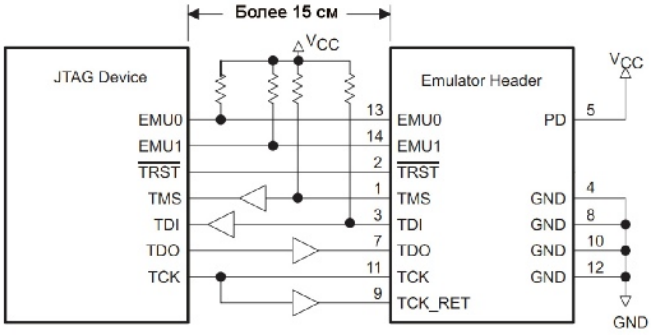

Figure 3-8. Buffered Emulation Signals

The EMU0 and EMU1 signals must have pull-ups to Vcc. The signal rise time of the pull-up resistors should be less than 10 µS. A 4.7k Ω resistor is suggested for most applications. EMU0-1 are I/O pins of the target device, however, they are inputs for the emulator only. These pins are used in multiprocessor systems to provide run/stop operations.
The emulator pod enables sequential termination of the TMS, TCK, and TDI signals. Figure 3-9 shows an application with the system test clock generated in the target system. The TCK signal is left unconnected in this application.
There are two reasons for having the target system generating the test clock:

- The emulator provides a 25-MHz test clock on default (the actual value can be adjusted in the configuration file). When using the target system test clock you can set the frequency to match your system requirements.
- Sometimes the test clock is required when the Emulator is switched off.

Figure 3-10 shows emulator mode without using return clocking (TCK_RET). Parameter configuration description is shown in p.3.6.4. Signal TCKR (TCK_RET) is optional in ARM20 connector and may be left unconnected in pcb. Example of such pcb type is «IAR KickStart Kit for TMS470». To work with such type of pcb it is required to use this type of connection and mode.

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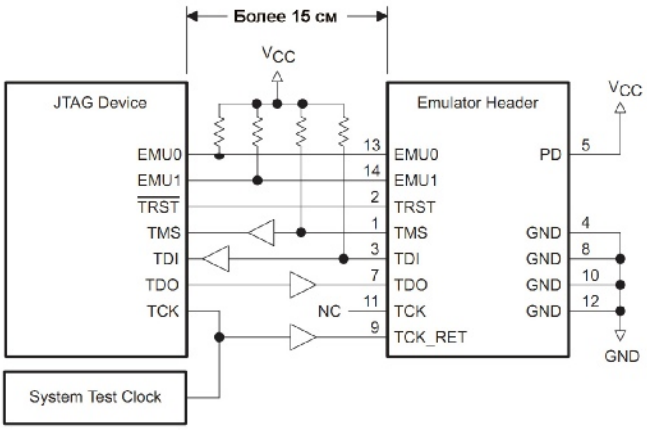


Figure 3-9. Target System Generates Test Clock

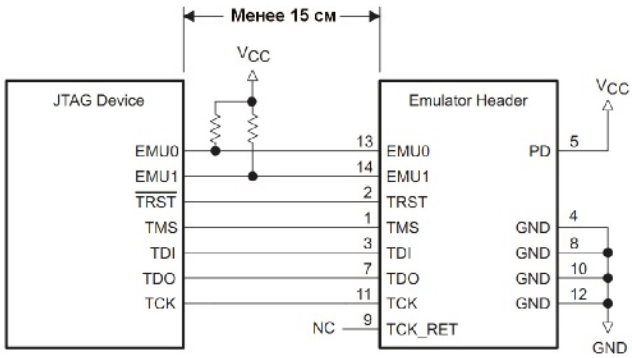


Figure 3-10. Work without return JTAG clocking (TCK_RET)

Figure 3-11 shows a typical multiprocessor configuration. This is a daisy chained configuration (TDO-TDI daisy-chained), that meets the minimum requirements of the IEEE 1149.1 specification. The emulation signals in this example are buffered to isolate the processors from the emulator and provide adequate control signal for the target system. One of JTAG test interface benefits is that you can slow down the test clock to eliminate timing problems.

Multiprocessor systems should meet the following requirements:

- The processor TMS, TDI, TDO and TCK signals are to be buffered to control timing skew better.
- The input buffers for TMS, TDI, and TCK should have pull-ups to Vcc. This will hold these signals at a required value if the emulator is switched off. A pull-up resistor of 4.7k Ω is suggested for most applications.

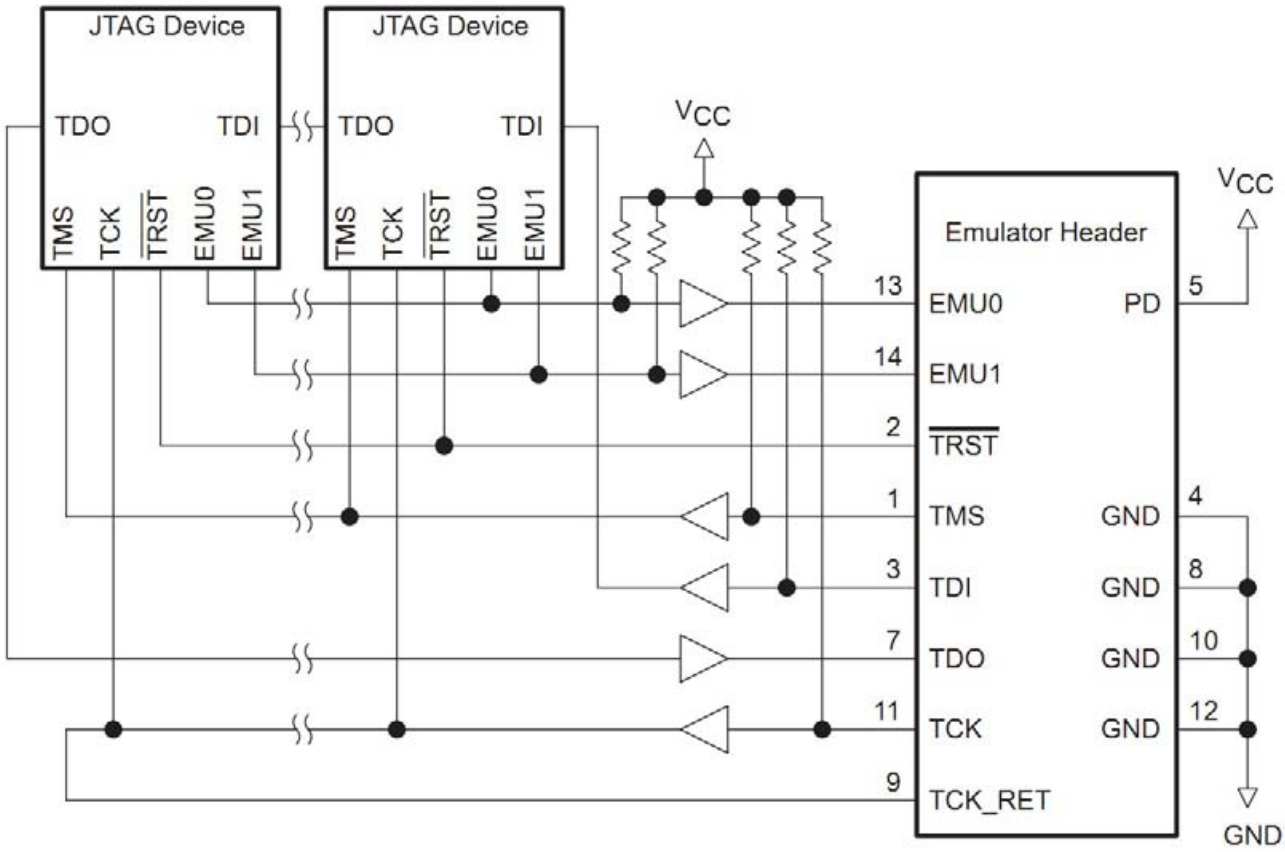
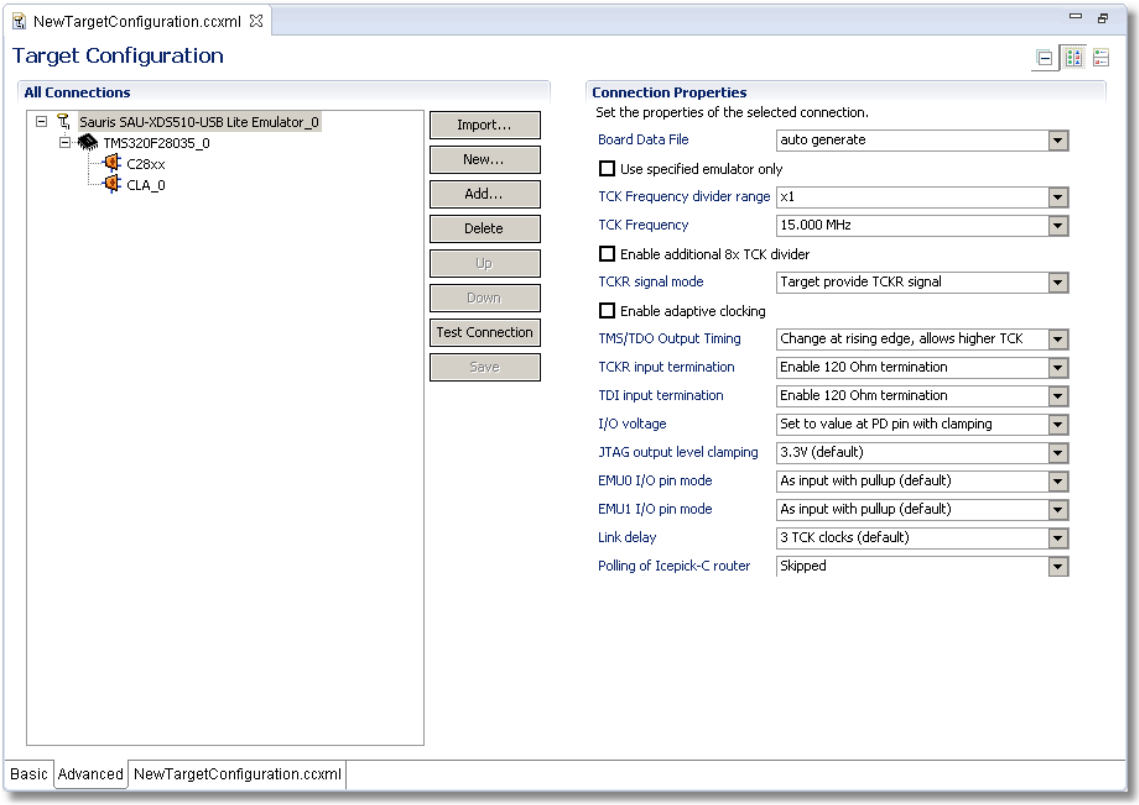


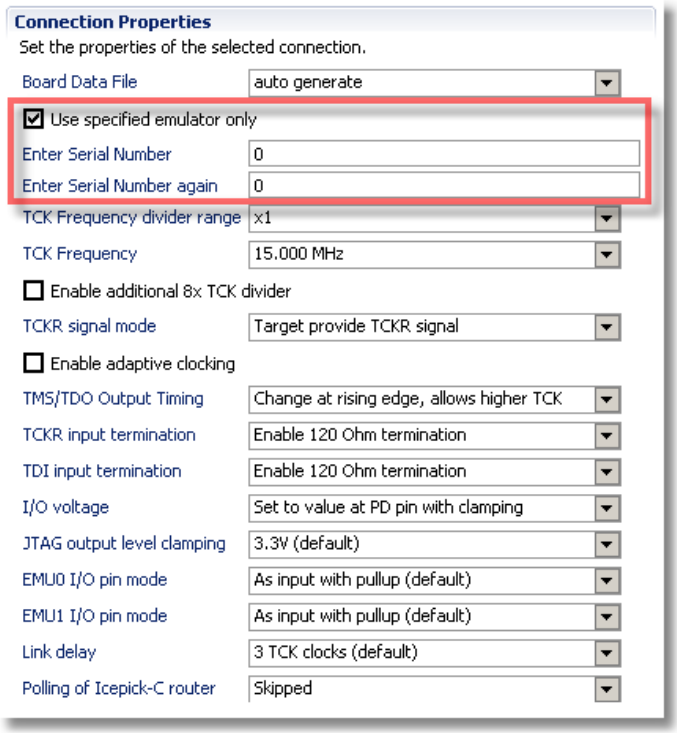
Figure 3-11. Multiprocessor Connections

3.6. JTAG-connection settings

The following emulator connection parameters can be configured in the tab "Advanced" of "Target Configuration" panel. On the tab you can set various parameters and conditions to ensure the correct emulator operation to debug the device. Below is a description of the available positions for adjustments in the integrated development environment Code Composer Studio v.6. For CCS 4.x and 5.x parameters are set similarly. For CC4.10 (for TMS320VC33), CCS 2.x and CCS3.x it is possible to change parameters by direct configuration file edit. Visit our forum for these IDEs parameter setting details.



3.6.1. Parameters for connection several emulators to one PC



Below you will find the parameters required for connecting several Emulators to one PC. The key factor is to link each connection to a definite Emulator by its serial number.
Select the "Advanced" tab in the "Target Configuration" editor. Select the connection. After that "Connections Properties" will appear on the right side. Set the parameter "Use specified emulator only" and after that enter the values into the "Enter Serial Number" and "Enter Serial Number again" fields.

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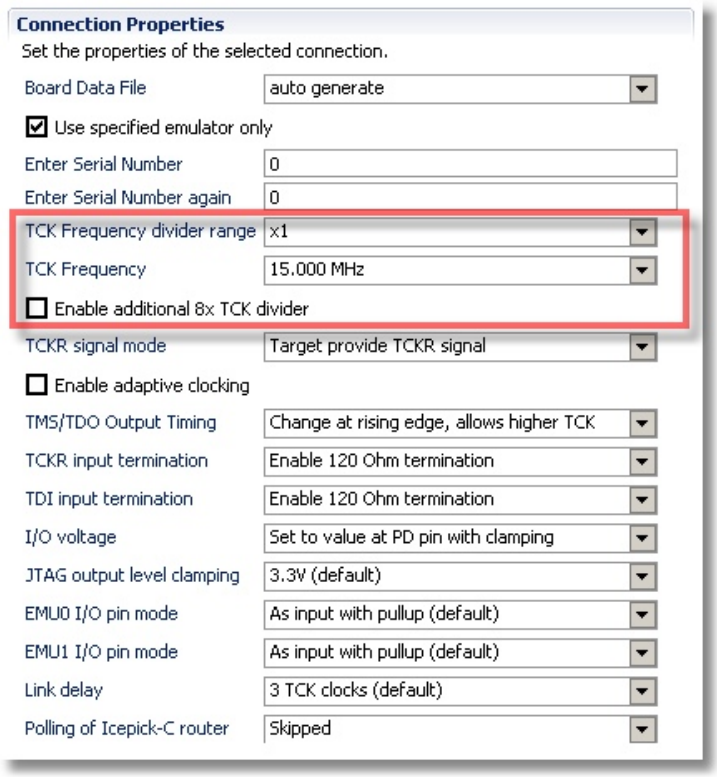
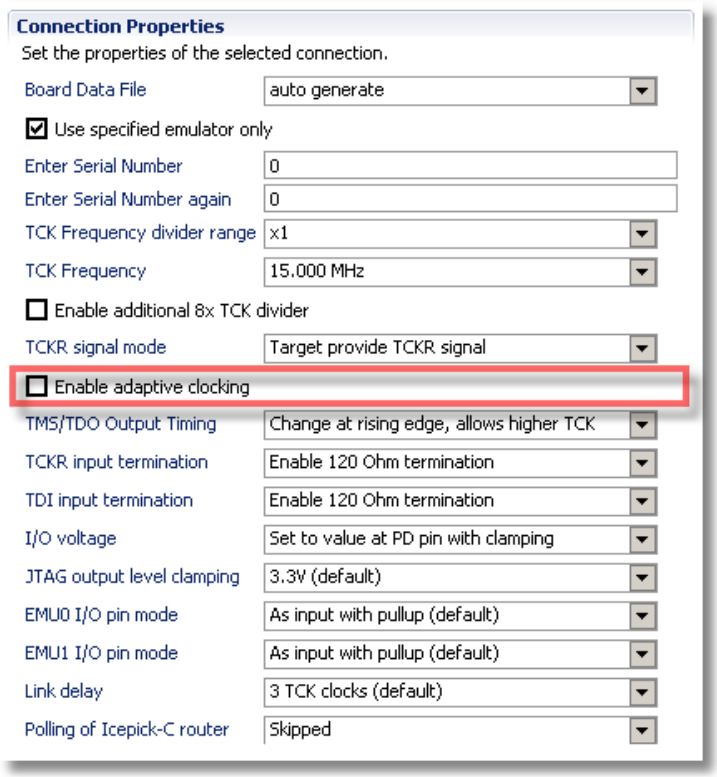
3.6.2. Parameters for setting TCK frequency



There are two ways to enable the clocking of the JTAG-chain. These are clocking at a fixed frequency and adaptive clocking. The fixed frequency can be used for most hardware where the maximum allowed TCK does not depend on the CPU frequency. The adaptive clocking is used for the devices that require dynamically changing TCK for operating – in these devices the TCK is based on the clock frequency of the CPU. DaVinci is an example of such a device – it includes ARM- and DSP-cores that have different clock frequency and the TCK in each moment depends on the frequency of the currently active core.

To set the TCK in the CCS select tab "Connections Properties" and set TCK Frequency Divider range and TCK Frequency. You can initiate an additional frequency divider by setting "Enable additional 8x TCK divider" parameter.

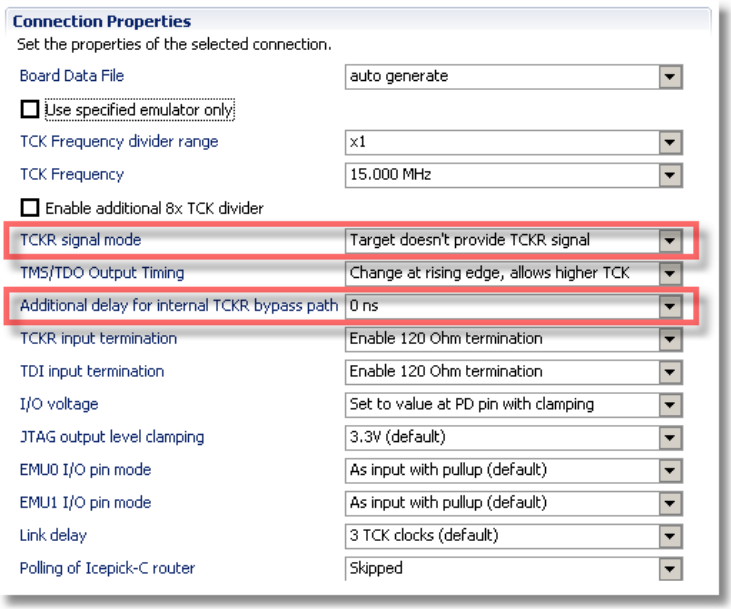
3.6.3. Adaptive clocking mode



On default TCK is generated by the emulator independently of the TCKR from the target. The TCK frequency is constant. But some processors require the TCK to be below some limit. The limit is set inside the processor and depends on the processor's own clock frequency, which can change considerably during the operating, e.g. because of PLL programming. Such processors have JTAG return clock frequency output gated by the required internal frequency. If this output is connected to emulator's TCKR input, the adaptive clocking mode allows the emulator to operate at the maximum frequency, that is possible for the processor. The reason is: in adaptive clocking mode the edge at the TCK is formed according to not only TCK, but also to the correspondence between TCKR-signal and the current TCK signal. The rising or falling edge will. Thus the rising or falling edge can never be generated before the previous rising/falling edge goes through TCK > TCKR circuit In this case maximum frequency is limited by divider. Adaptive clocking mode is usually used with ARM processors.

To set Adaptive clocking mode check the "Enable adaptive clocking" parameter in the connection properties.

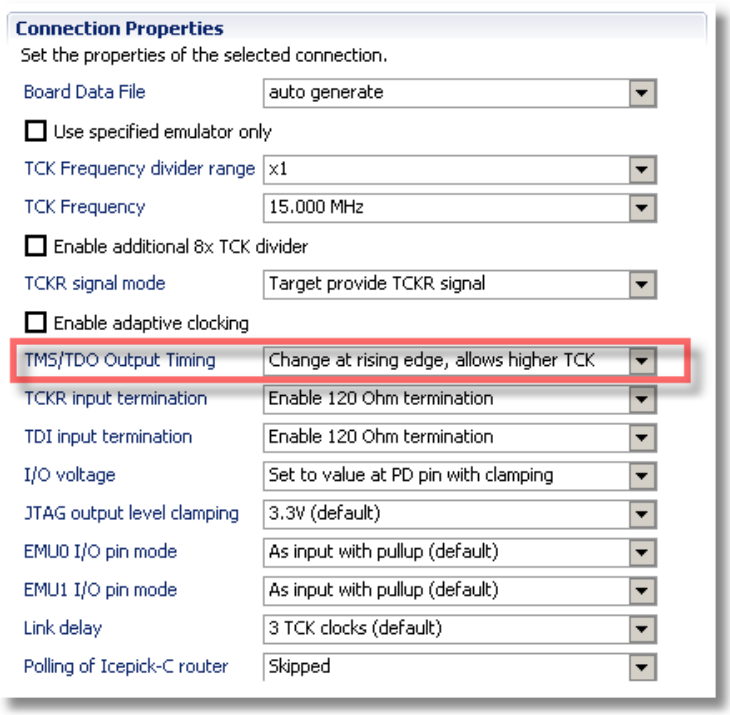
3.6.4. Functioning without return clocking (TCKR).



In some cases the system has to operate without return clocking signal (TCKR), for example when operating with ARM JTAG where TCKR signal is optional. Thereto there is a bypass way for the signal TCK -> TCKR beside all outside circuits. This way provides approximately the same delay as outside circuit does when it includes standard cable and 5 cm length of TCK->TCKR. There is an opportunity to increase this delay by the 4,8 ns (1/210 MHz) step.

To enable operating without return clocking mode set "Target doesn't provide TCKR signal" in the "TCKR signal mode" parameter. After that set "Additional delay for internal TCKR bypass path".

3.6.5. TMS and TDO emulator signals output buffers' clocking mode.



Data update may occur on both signal TCK_RET falling edge and on rising edge. While outputting on falling edge the work complies with IEEE1149.1. While outputting on rising edge it is possible to use higher clock TCK. While emulator is working in Adaptive Clocking mode with processors containing ARM9 or ARM11 core, use falling edge TDO/TMS outputting. To get maximum emulation speed use rising edge TDO/TMS outputting with maximum TCK clock on which system works stable.

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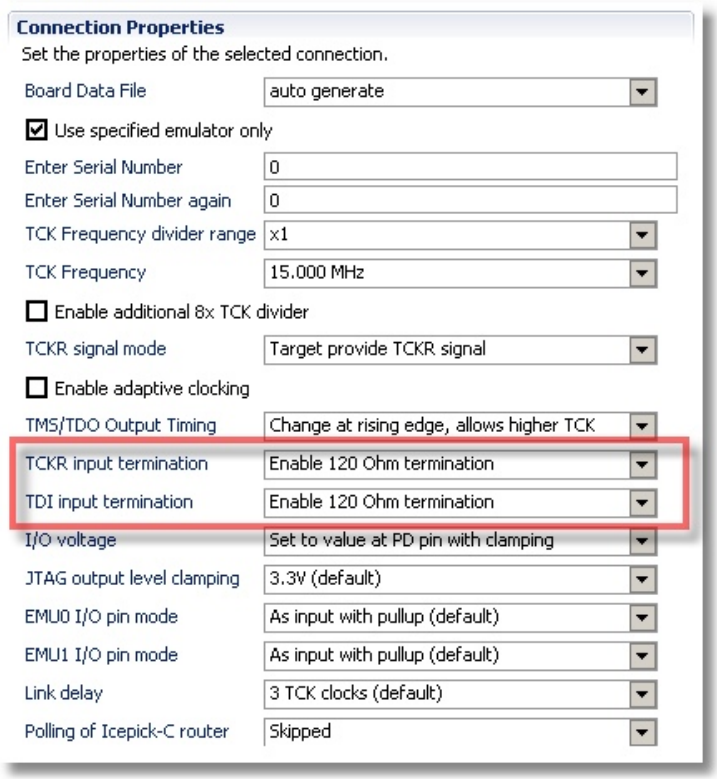
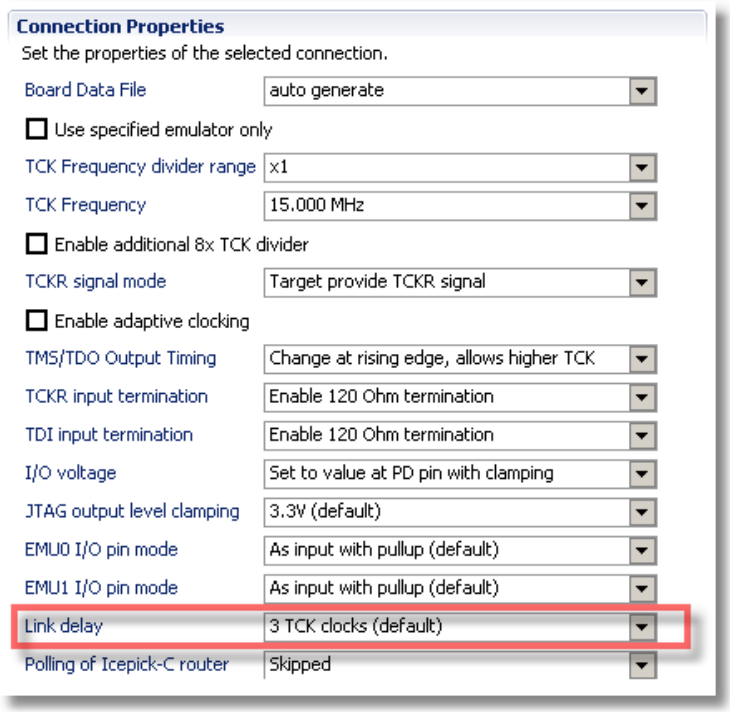
3.6.6. Impedance matching circuits control



There is an opportunity to connect the impedance matching circuits to TCKR and TDI pins to improve this signals quality. This connection is on by default.

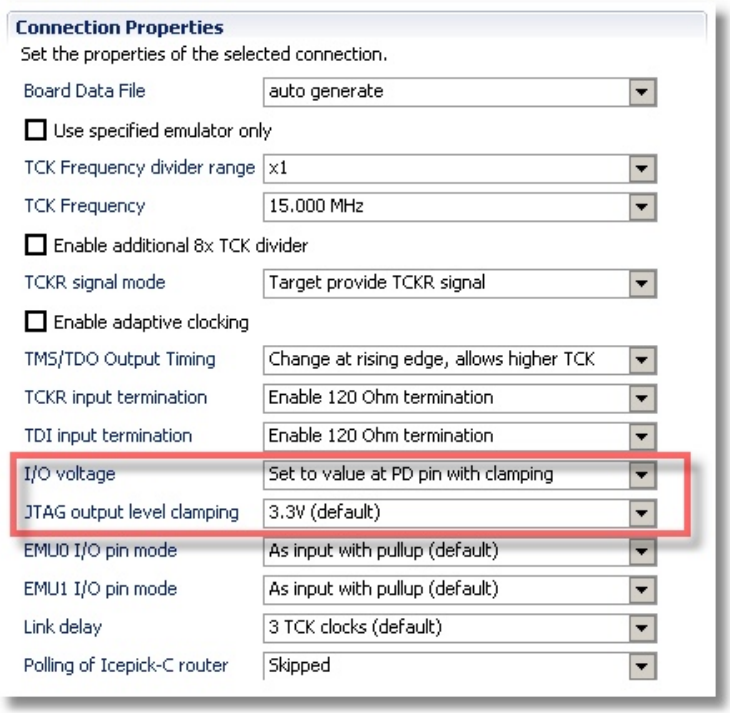
To connect the impedance matching circuits to TCKR and TDI you should set appropriate value in "TDI input termination" or "TCKR input termination" parameters.

3.6.7. Connection tweaking

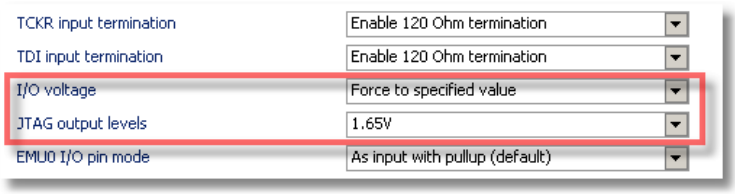


("Link delay"). This parameter sets the number of TMS and TDO delay cycles after they are generated in the emulator by JTAG-controller and before they come to the processor pins.
Minimum value is 3 because of the count of synchronization flip-flops inside the emulator. If the delay of TMS/TDO generated from the rising edge of TCKR-signal exceeds one cycle of TCKR, the Link Delay should be increased by one, thus the value is to be 4. If the delay exceeds two cycles, the Link Delay is to be increased by 2.

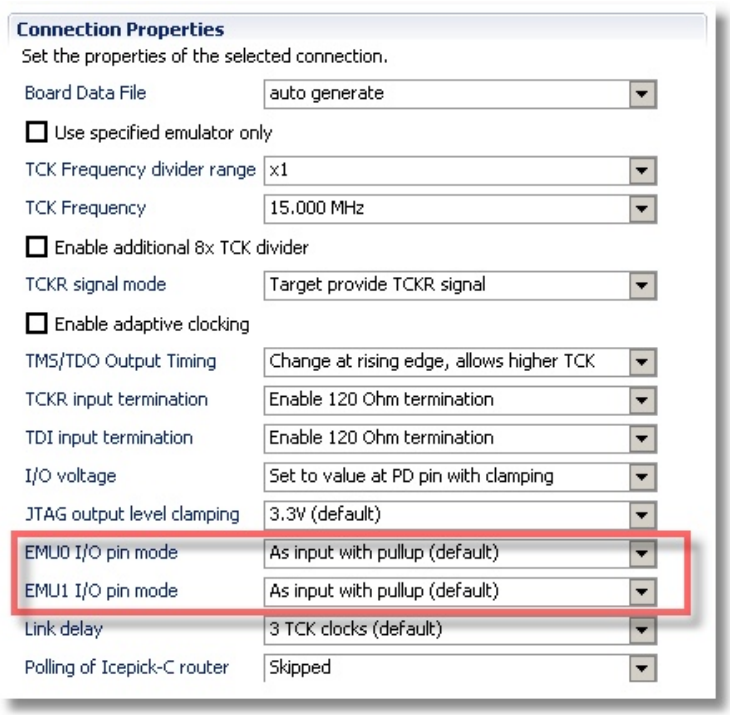
3.6.8. JTAG output level clamping



It is possible to limit JTAG signal by value smaller or equal to voltage on PD pin. For example, in case of 5V PD pin voltage, 3.3, 2.5 processors compatibility is possible. Force setting JTAG signal level is possible. To do this it's required to set "I/O voltage" parameter to "Force to specified value". After that it is possible to force set "JTAG output levels" parameter value.



3.6.9. EMU0/1 pin



EMU pins are bidirectional and set the JTAG operation mode. They can be used for transmission of data and event. The emulator can be used not only as inputs for the data/events, and as outputs with arbitrary values, which actually set through "EMU I/O pin mode"

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